IN THE CLAIMS:

Amend claims 1 and 3-5, cancel claims 2 and 6 without prejudice or admission, and add new claims 7-12 as shown in the following listing of claims, which replaces all previous listings and versions of claims in this application.

1. (currently amended) A vertical MOS transistor comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial growth layer of the first conductivity type ~~which is~~ formed on the semiconductor substrate;

a body region of a second conductivity type ~~which is~~ formed on the epitaxial growth layer;

a heavily doped body contact region of the second conductivity type ~~which is~~ formed on a part of a surface of the ~~second conductivity type~~ body region;

a heavily doped source region of the first conductivity type ~~which is~~ formed on a part of the surface of the ~~second conductivity type~~ body region that is not covered with the heavily doped body contact region;

a silicon trench piercing the ~~second conductivity type~~ body region and the ~~first conductivity type~~ heavily doped source region to reach an inner part of the ~~first conductivity type~~ epitaxial growth layer;

a gate insulating film formed along ~~walls~~ side wall surfaces and bottom surfaces of the silicon trench;

a heavily doped polycrystalline silicon gate buried in the silicon trench over the gate insulating film to a level of the ~~first conductivity type~~ heavily doped source region ~~while surrounded by the gate insulating film~~;

an intermediate insulating film formed on the heavily doped polycrystalline silicon gate in the silicon trench to reach a surface of the semiconductor substrate;

an insulator disposed on the side walls of the silicon trench and above the heavily doped polycrystalline silicon gate;

a metallic source electrode having a flat surface ~~to be~~ in contact with the intermediate insulating film, the heavily doped source region, and the heavily doped body contact region; and

a metallic drain electrode connected to a rear surface of the semiconductor substrate.

2. (canceled).

3. (currently amended) A vertical MOS transistor according to claim ~~2, wherein~~ 1; wherein the insulator ~~provided~~ disposed on the side walls of the silicon trench ~~is~~ comprises a silicon nitride film.

4. (currently amended) A vertical MOS transistor according to claim ~~3, wherein~~ 3; wherein the heavily doped polycrystalline silicon gate is buried ~~in the silicon trench is~~ 0.5 μm to 1.0 μm down from ~~the~~ a top of the silicon trench.

5. (currently amended) A vertical MOS transistor according to claim 1; wherein ~~2, wherein~~ the heavily doped polycrystalline silicon gate is buried ~~in the silicon trench is~~ 0.5 μm to 1.0 μm down from ~~the~~ a top of the silicon trench.

6. (canceled).

7. (new) A vertical MOS transistor comprising:

a semiconductor substrate;

an epitaxial growth layer disposed on the semiconductor substrate;

a body region disposed on the epitaxial growth layer;

a heavily doped body contact region disposed on a part of a surface of the body region;

a heavily doped source region disposed on a part of the surface of the body region on which the heavily doped body contact region is not disposed;

a silicon trench extending through the heavily doped source region and the body region and extending into the epitaxial growth layer, the silicon trench having sidewall surfaces and a bottom surface;

a gate insulating film disposed on the sidewall and bottom surfaces of the silicon trench;

a heavily doped polycrystalline silicon gate disposed in the silicon trench over the gate insulating film and extending below a surface formed by the body region and the heavily doped body contact region;

an intermediate insulating film disposed on the heavily doped polycrystalline silicon gate in the silicon trench so as to reach the surface formed by the body region and the heavily doped body contact region; and

an insulator disposed on the sidewalls of the silicon trench and above the heavily doped polycrystalline silicon gate.

8. (new) A vertical MOS transistor according to claim 7; further comprising a metallic source electrode having a generally planar surface disposed in contact with the intermediate insulating film, the heavily doped source region, and the heavily doped body contact region.

9. (new) A vertical MOS transistor according to claim 8; wherein the surface of the semiconductor substrate comprises a first surface; and further comprising a metallic drain electrode connected to a second surface of the semiconductor substrate opposite to the first surface thereof.

10. (new) A vertical MOS transistor according to claim 7; wherein each of the semiconductor substrate, the epitaxial growth layer, and the heavily doped source region have a first conductivity type; and wherein each of the body region and the heavily doped body contact region have a second conductivity type different from the first conductivity type.

11. (new) A vertical MOS transistor according to claim 7; wherein the insulator comprises a silicon nitride film.

12. (new) A vertical MOS transistor according to claim 7; wherein a distance from the surface formed by the body region and the heavily doped body contact region to an upper surface of the heavily doped polycrystalline silicon gate disposed in the silicon trench is in the range of 0.5 μm to 1.0 μm.